

## **FULL SUITE BUNDLE**

<b>University Bundle - Full Suite</b>	
<b>The Custom Integrated Circuit Bundle</b>	
<b>Design Environment</b>	
Virtuoso® AMS Designer Environment	70000
Virtuoso® Analog Design Environment - XL	95210
<b>Design Entry</b>	
Virtuoso(R) Simulation Environment	206
Cadence® SKILL Development Environment	900
Virtuoso® Schematic VHDL Interface	21060
Virtuoso® Schematic Editor VerilogR Interface	21400
Virtuoso® Schematic Editor - XL	95115
Virtuoso® Analog Oasis Run-Time Option	32100
Cadence(R) Design Framework Integrator's Toolkit	12141
<b>Layout</b>	
Virtuoso® Layout Suite - GXL1	95321
Cadence® Chip Assembly Router2	3300
<b>Physical Verification</b>	
Assura™ Design Rule Checker	72110
Assura™ Layout vs. Schematic Verifier	72120
Virtuoso® QRC Extraction - XL	QRCX300
Virtuoso® Advanced Analysis GXL option	QRCX310
Assura™ Graphical User Interface Option	72140
Assura™ Multiprocessor Option	72150
Pcell Generator	PASPCG
Graphical Technology Editor	PASGTE
Cadence® Physical Verification System Design Rule Checker XL	96210
Cadence® Physical Verification System Layout vs. Schematic Checker XL	96220
Cadence(R) Design Framework II	111
<b>Circuit Simulation</b>	
Virtuoso® Analog Design Environment - GXL	95220
Virtuoso® Spectre® Circuit Simulator	38500
Virtuoso® UltraSim Full-chip Simulator MMSIM72	33500
Virtuoso® Spectre® RF Simulation Option for	38520
Virtuoso® RelXpert	33580
AMS Designer with Flexible Analog Simulation	70020
Virtuoso® Multi-mode Simulation with AP Simulator	90003
<b>Interfaces</b>	
Cadence® Design Framework Integrator's Toolkit	12141
<b>Digital Integrated Circuits Bundle</b>	
<b>Formal Verification</b>	
Encounter™ Conformal - CONFRML91	GXL CFM300
<b>Synthesis</b>	
Encounter™ RTL Compiler - XL RC 101	RC200

Encounter™ RTL Compiler - GXL option RC 101	RC300
Encounter™ RTL Compiler with physical RC 101	RC400
<b>Test</b>	
Architect Advanced Option to RC ET91	ET021
Encounter™ True Time Test Advanced ET91	ET023
Encounter™ Diagnostics Engine - XL ET91	ET009
<b>Chip Planning</b>	
Cadence® InCyte Chip Estimator XL CICE40	CPS200
<b>Verification Bundle</b>	
Functional Verification	
Cadence® Simulation Analysis Environment (SimVision) IUS82	25010
Incisive™ Enterprise Simulator 29651 IES82	29651
Enterprise Simulator - XL Interface for MTI IES82	29661
Enterprise Simulator - XL Interface for VCS IES82	29671
Incisive™ Formal Verifier IFV82	23560
Incisive™ Enterprise Verifier – XL IFV82	IEV101
Incisive™ Software Extensions INCISV102	ISX100
Virtuoso® AMS Designer Verification Option INCISV102	70030
<b>Verification Process Automation</b>	
Incisive™ Enterprise Manager EMGR82	EMG100
Incisive™ VIP Portfolio VI	VIP100
Litho Physical Analyzer	LPA108
Litho Electrical Analyzer	LEA108
<b>Design for Manufacturing</b>	

VoltageStorm (transistor) ANLS62	VST1
Encounter Power System - L ETS91	EPS100
Signal Integrity	
Encounter™ Timing System - XL ETS91	FE725
Pacific Static Noise Analyzer for Custom Digital ICs PACIFIC61	CM00100
Encounter™ Timing System - L ETS91	FE625
Encounter™ Library Characterizer- XL ETS91	ELC200
Silicon Virtual Prototyping	
Encounter™ Digital Implementation System - XL EDI91	EDS200
Encounter™ Low Power GXL Option EDI91	EDS10
Encounter™ Advanced Node GXL option EDI91	EDS30
Digital System-In-Product (SiP)1	
Cadence® SiP Digital Si - XL SIP215 SPB163	SIP215
Silicon-Package-Board Products	
PCB Design and Layout	
Allegro® PCB Librarian - XL PX3500 SPB163	PX3500
Allegro PCB Designer	PA3100
Allegro PCB High-Speed Option	PA3110
Allegro PCB Miniaturization Option	PA3120
Allegro PCB Routing Option	PS3500
Allegro Design Authoring High-Speed Option	PA1410
PCB High-Speed Analysis	
Allegro® PCB SI - XL PX3100 SPB163	PX3100
IC Packaging	
Cadence® SiP Layout – XL SIP225 SPB163	SIP225
Simulation	
Allegro® AMS Simulator1 PS2200 SPB163	PS2200